Remarks

Claims 14-23 and 33-40 are pending.

Claims 14-19, 21-23 and 34-40 stand rejected.

Claim 20 is objected to.

Claims 14, 20 and 33 have been amended.

Claim 68 has been added.

Claims 14-23, 33-40 and 68 an are submitted herein for review.

No new matter has been added.

In paragraph 1 of the Office Action, the Examiner has objected to the title as not being sufficiently descriptive. Applicants have amended the title accordingly and respectfully request that this objection be withdrawn.

In paragraph 3 of the Office Action, the Examiner has rejected claims 14-19 and 33-37 as being unpatentable over Bowes et al. (U.S. Patent No. 5,655,151) in view of Normoyle (U.S. Patent No. 5,884,100). In paragraphs 5-7 the Examiner has also rejected dependent claims 15-19, 34-37 as unpatentable over Bowes in view of Normoyle. In paragraph 8 of the Office Action the Examiner has rejected claims 21-23 and 38-40 as being unpatentable over Bowes in view of Normoyle, further in view of Handy (The Cache Memory Book of Jim Handy).

In paragraph 10 the Examiner has indicated that dependent claim 20 would be allowable

if re-written in independent format.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

The present invention as claimed in independent claim 14 is directed to an information processing system, having a plurality of modules including a processor, a cache memory, a main memory and a plurality of I/O devices, a data streamer for performing data transfer operations between the modules.

The information processing system maintains a channel state memory configured to store a first allocated channel information, including data addresses, corresponding to a data transfer operation from a source module to the data streamer. A second allocated channel information, including data addresses, is stored, corresponding to the data transfer operation from the data streamer to a destination module.

A buffer memory is allocated to the data transfer operation for receiving data provided by the source module in accordance with the first allocated channel information and providing the received data to the destination module in accordance with the second allocated channel information.

A buffer state memory is configured to store a relationship which determines that the first channel information and the second channel information and the buffer memory are used in the data transfer operation.

In this arrangement the present invention has two channels selected during a data transfer. A first allocated channel information corresponding to a data transfer operation from a source

module to a data streamer and a second allocated channel information corresponding to the transfer operation from the data streamer to a destination module. The information relating to the two channels is stored in a channel state memory (704). According to the structure as claimed, each of the first and second channel information includes data addresses, corresponding to a data transfer operation from a source module to a destination module.

As noted in the accompanying portion of the specification, in the last two paragraphs of page 36 and the first paragraph on page 37, in this arrangement of the present invention as claimed, the system is able to configure an address for each selected channel, resulting in an increased efficiency in memory (address space) to memory (address space) transfers.

The relationship stored in buffer state memory relates IDs to one another of the two channels, such as for example, the ID of the first channel (BIT 59:54) of buffer state memory and the ID of the second channel (BIT 53:48) of the buffer state memory. See Table 23, pages 66-67 of the specification.

In the rejection of claims 14 and 33, the Examiner, citing Bowes, asserts:

> "a channel state memory configured to store a first allocated channel information corresponding to a data transfer operation from a source module to the data streamer, and further configured to store second allocated channel information corresponding to the data transfer operation from the data streamer to a destination modules (see line 61 of column 6 to line 34 of column 7; Note the register set is the channel state memory
>
> a buffer memory allocated to the data transfer operation for receiving data provided by the source module in accordance with the first allocated channel information and providing the received data to the destination module in accordance with the second allocated channel information (see line 61 of column 6 to line 34 of column 7; Note the FIFO is the buffer memory)."

However, as noted in column 7, lines 36-41 of Bowes:

> "The use of a multiple register set architecture, as described above, allows the DMA controller 218 to chain two transfers together. That is, each register set can be programmed for a transfer and the transfer for the second register set will begin immediately following the completion of the first register set's transfer."

Thus, it is disclosed in Bowes, that DMA controller 218 chains two transfers together by using a multiple set architecture. Furthermore, there is a disclosure of the method that each register set can be programmed for a transfer, and that the transfer for the second register will begin immediately following the completion of the first register.

Again as noted in Table 2 of Bowes, the 9 DIR Bit No. teaches:

> "Direction. This bit indicates in which direction the DMA channel should operate. If set, then the DMA channel should read from the I/O device to memory. If not set, then the DMA channel should write from memory to the I/O device. When read, this bit always reflects the current read/write state for the DMA channel."

Consequently, the structure register set according to the Bowes description is configured as one register set used for one transfer between memory and the I/O. This is in contrast to the present invention as claimed in independent claims 14 and 33 which employs two channels for a memory to memory transfer.

As such, Applicants respectfully submit that the cited Bowes reference does not teach or suggest the elements of the claimed invention as indicated by the Examiner. For example, there is no teaching or suggestion in Bowes that discloses a channel state memory configured to store a first allocated channel information, *including data addresses*, corresponding to a data transfer operation from a source module to the data streamer, and further configured to store a second allocated channel information, *including data addresses*, corresponding to the data transfer

operation from the data streamer to a destination module.

Likewise, the Bowes reference does not teach or suggest a buffer state memory configured to store a relationship which determines that the first channel information and the second channel information and the buffer memory is used in the data transfer operation.

It is noted that the Examiner did not cited to either Normoyle or Handy in this respect. However, Applicants submit that neither of these reference teach or suggest such elements either. For example, there is no teaching or suggestion in either Normoyle or Handy that discloses a channel state memory configured to store a first allocated channel information, *including data addresses*, corresponding to a data transfer operation from a source module to the data streamer, and further configured to store a second allocated channel information, *including data addresses*, corresponding to the data transfer operation from the data streamer to a destination module.

Likewise, the Normoyle and Handy references do not teach or suggest a buffer state memory configured to store a relationship which determines that the first channel information and the second channel information and the buffer memory is used in the data transfer operation. Thus, none of the cited references, either alone or in combination with one another, teach or suggest all of the elements of the present invention as claimed.

As such, Applicants respectfully request that the rejection of independent claims 14 be withdrawn. Method claim 33 should also be considered allowable for the same reasons set forth in the forgoing remarks. Also, as claims 15-19, 21-23 depend from claim 14 and claims 34-40 depend from claim 33 these claims should be allowed for the same reasons as set forth above.

Applicants further note that allowable claim 22 has been re-written in independent form

and new claim 68 teaches a method of operating a system having similar elements to that in claim 20.

In view of the forgoing, Applicants respectfully submit that the pending claims 14-23 and 33-40 are in condition for allowance, the earliest possible notice of which is earnestly solicited. If the Examiner feels that an interview would facilitate the prosecution of this Application they are invited to contact the undersigned at the number listed below.

Respectfully submitted,

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